Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. MR**
2. **Q0**
3. **D0**
4. **D1**
5. **Q1**
6. **D2**
7. **Q2**
8. **GND**
9. **CP**
10. **Q3**
11. **D3**
12. **Q4**
13. **D4**
14. **D5**
15. **Q5**
16. **VCC**

**.052”**

****

**.065”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .052” X .065” DATE: 6/13/18**

**MFG: Texas Inst. THICKNESS .014” P/N: 54HC174**

**DG 10.1.2**

#### Rev B, 7/1